The Importance of Ballistic Resistance in the Modeling of Nanoscale InGaAs MOSFETs

Jianqiang Lin, *Member, IEEE*, Xiaowei Cai, *Student Member, IEEE*,
Dimitri A. Antoniadis, *Life Fellow, IEEE*, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— Physics-based transistor models are important for technology projections and circuit simulations. To date, there has been little discussion on the incorporation of ballistic effects in transistor models. Recent experimental studies have revealed the significance of ballistic transport in the electrical characteristics of nanometer-scale InGaAs MOSFETs with ultra-low external resistance. Without proper accounting for the ballistic resistance and its gate voltage dependence, the access resistance to the intrinsic device cannot be accurately determined, and any physics-based transistor modeling is bound to fail. In this letter, we show that the MIT Virtual Source model, which natively captures ballistic transport physics, correctly incorporates the impact of ballistic resistance. As a result, it accurately models the electrical characteristics of self-aligned nanoscale InGaAs MOSFETs, an excellent model system for near-ballistic transistors, over a broad operational range. We also show that the success of the model development effort crucially relies on the correct extraction of the external source and drain resistance, R_{sd}, from experimental measurements.**

***Index Terms*— III-V, quantum-well MOSFETs, ballistic mobility, ballistic resistance, near-equilibrium transport.**

I. Introduction

THE continuous scaling of CMOS transistors has resulted in device dimensions comparable to or smaller than the carrier mean-free-path, λ. These devices operate in the so-called quasi-ballistic regime [1], [2]. The use of alternative channel materials with low effective mass, such as InGaAs, brings along relatively large λ values and pushes transistor operation even closer to the ballistic limit.

In the analysis of quasi-ballistic nanoscale transistors, it has been found useful to introduce the notion of *ballistic mobility* which accounts for ballistic carrier transport over the finite length of the channel under a low longitudinal electric field [3]. Shur showed that the channel-length-dependent ballistic mobility, μ_B, in combination with the mean-free-path-dependent, i.e. scattering-limited, effective mobility, μ_{eff}, results in a length-dependent apparent carrier mobility, μ_{app}, that is smaller than either [3], $\mu_{app}^{-1} = \mu_{eff}^{-1} + \mu_B^{-1}$. In transistors with low external resistance and under near-equilibrium conditions, the ballistic mobility can manifest itself as an additional length-independent *ballistic resistance* that can be comparable to the value of R_{sd}, which is the sum of external source resistance, R_s, and external drain resistance, R_d, and accounts for the total access path to the channel. The ballistic resistance depends on the non-degenerate unidirectional thermal velocity, the thermal voltage and the reduced surface potential, as shown in [4]. Because both the ballistic resistance and the external source and drain resistance are channel-length-independent, usual extraction methods fail to distinguish between them and lead to an overestimation of R_{sd}. Recent experimental analysis of III-V MOSFETs [4] and Si ETSOI MOSFETs [5] in the low-field regime have shown consistency with those formulations, but the incorporation of this physics into transistor analytical models has not been examined. This letter focuses on the challenges involved and shows that proper treatment of the ballistic resistance is crucial for the correct modeling of quasi-ballistic transistors.

The MIT Virtual Source (MVS-2) model, a physics-based analytical model, includes the ballistic mobility inherently into its self-consistent formulation of the transmission-theory [6], [7]. The MVS model is built on a philosophy of minimizing the number of model parameters while still maintaining the capability to accurately describe transistor behavior across the full operational range. The MVS model has evolved considerably from its first implementation [6] to successfully describe carrier transport in nanoscale silicon FinFETs [5] and InGaAs High-Electron-Mobility Transistors (HEMTs) [8], among others.

In this letter, we investigate the use of the MVS model to describe the behavior of nanometer-scale self-aligned InGaAs MOSFETs that exhibit very small external resistance, a case where the ballistic resistance is of particular importance. We show that the MVS model properly accounts for ballistic effects and accurately reproduces the transistor characteristics provided that the value of the external resistance is extracted with proper consideration of ballistic effects. Without this, significant discrepancies emerge.

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J. Lin is with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA, and also with the Argonne National Laboratory, Argonne, IL 60439 USA (e-mail: linj@anl.gov).

X. Cai, D. A. Antoniadis, and J. A. del Alamo are with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: alamo@mit.edu).

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II. MVS Model of InGaAs MOSFETs

We have studied the modeling of self-aligned InGaAs Quantum-well MOSFETs with a structure and fabrication process described in [9], [10]. The channel thickness is 7 nm. Devices with effective gate lengths, L_{eff}, between 70 and 650 nm were analyzed. These transistors display excellent performance characteristics with a peak g_m of 2.9 mS/μm at $V_{ds} = 0.5$ V in an $L_{eff} = 70$ nm device. The devices were characterized at room temperature through I-V and split C-V measurements following [4]. To minimize device degradation under current and bias stress [11], the maximum bias was limited so that the device current did not exceed 0.6 mA/μm.

The critical parameters for the MVS modeling effort in this work and their extraction are discussed next. The model for the channel charge at the virtual source is based on the 2D density of states accounting for band non-parabolicity on the effective mass and Fermi-Dirac statistics. An equivalent gate oxide thickness, t_{ox}, of 0.5 nm is obtained from the physical thickness of 2.5 nm and the dielectric constant of HfO_2, which is equivalent to an oxide capacitance, C_{ox}, of 6.9 μF/cm^2. From the MVS capacitance simulations, it is found that the quantum capacitance that mainly depends on the effective mass of electrons in the channel, m_e^*, plays a dominant role on the device C-V characteristics. In comparison, the impact of t_{ox} variation (for such a thin gate oxide) on the C-V characteristics is relatively small. In this model, the value of m_e^* is the only tuning parameter (without varying the non-parabolicity parameter). We extract m_e^* by matching the experimental split-C-V characteristics of a long-channel device with $L_{eff} = 650$ nm at f=100 MHz with $V_{ds} = 0$ V. As Fig. 1a shows, the use of an electron effective mass $m_e^* = 0.041 m_o$ reproduces the measured C-V characteristics rather well by the analytical charge model in MVS [7]. This value is consistent with other studies of InGaAs channel transistors [7], [12]. Once m_e^* is determined, the electron injection velocity can be calculated taking into account carrier degeneracy, according to the MVS formulation [7].

Separately, the apparent mobility, μ_{app}, was extracted in the $L_{eff} = 650$ nm device from combined I-V and C-V measurements in the linear regime under the assumption that R_s and R_d have negligible effect at such large L_{eff}. μ_{app} is plotted as a function of carrier concentration, N_s, in the channel as black dots in Fig. 1b. The apparent mobility results from the Matthiessen's rule combination of the ballistic mobility, μ_B, and the L_{eff}-independent scattering-limited mobility, μ_{eff}. We can extract μ_B following the procedure in [4] involving multiple channel length devices. As shown in Fig. 2, this mobility is extracted from the slope of R_{on} (at very low $V_{ds} = 0.01$ V) vs. L_{eff} measured for multiple devices at different values of gate overdrive, and hence N_s. μ_{eff} is also graphed in Fig. 1(b) and serves as input to the MVS model in the form of a look-up table.

Focusing now on the $L_{eff} = 70$ nm device at low V_{ds}, the threshold voltage is experimentally determined to be $V_t = 25$ mV. To describe short channel effects, the drain-induced barrier lowering, DIBL, parameter value is 125 mV/V, obtained by fitting the output and subthreshold characteristics

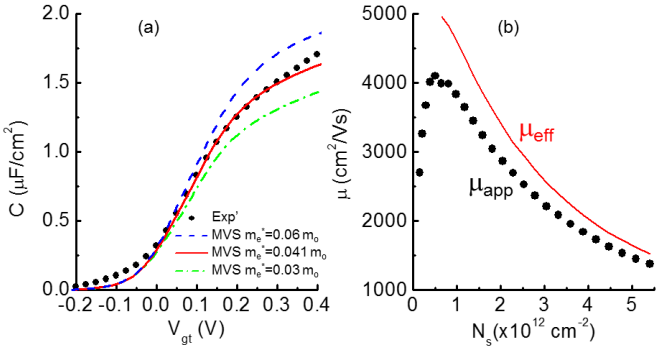

Fig. 1. (a) Normalized capacitance-voltage characteristics from measurement on long-channel device and the MVS analytical charge model with different electron effective mass. (b) Apparent mobility extracted in a device with $L_{eff} = 650$ nm and the field-effect mobility extracted by the method described in [4].

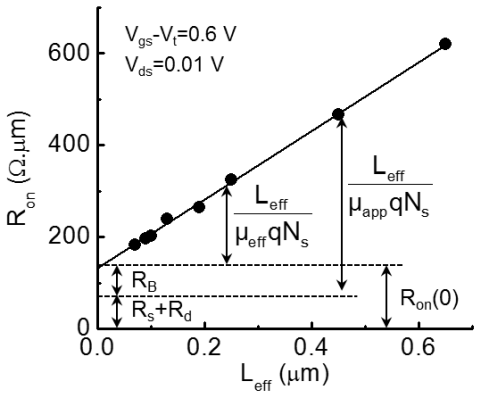

Fig. 2. R_{on} vs. L_{eff} under high $V_{gs} - V_t$. $R_{on}(0)$ is the y-intersection of the fitted straight line of R_{on} vs. L_{eff}. $R_{on}(0)$ is the sum of R_B and R_{sd}.

in Figs. 3a and 3c. Similarly, the experimental subthreshold swing is described through a non-ideality factor $n_o = 1.6$ due to the presence of interface states. A detailed explanation of DIBL and n_o in MVS are given in [7]. The deviation of experiment from model at negative V_{gs} at $V_{ds} = 0.5$ V in Fig. 3c is caused by band-to-band tunneling and a floating body bipolar effect [13] which are not captured in MVS.

Finally, the values of the external resistances, R_{sd}, need to be determined. Following the procedure in [4] this is also based on measurements of R_{on} vs. L_{eff}, as shown in Fig. 2 where the ON resistance at $L_{eff} = 0$, denoted as $R_{on}(0)$, is extracted as 130 $\Omega.\mu$m for a gate overdrive of 0.6 V.

In conventional transistor models, $R_{on}(0)$ is considered to be the sum of the source and drain resistances, i.e. $R_{on}(0) = R_{sd} = R_s + R_d$. Assuming a symmetric device, this implies that $R_s = R_d = 65$ $\Omega.\mu$m. If we follow this conventional approach to model the $L_{eff} = 70$ nm device, the MVS model yields results that are shown in dashed lines (blue) in Figs. 3 a - c. Clearly, the simulations fail to describe the measured electrical characteristics of the transistor (black dots). The model substantially underestimates the current drive of the transistor.

In the presence of ballistic transport, we have shown that $R_{on}(0)$ can significantly overestimate R_{sd} due to the presence of the ballistic resistance, R_B. R_B and μ_B are directly related, as discussed in [4]. In order to correctly extract $R_s + R_d$, R_B

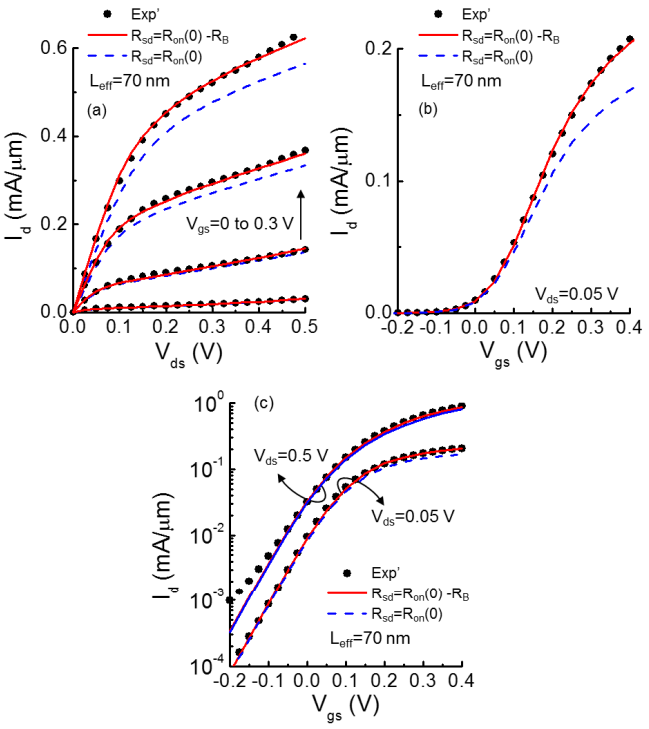

Fig. 3. (a) Output $I_d - V_{ds}$, (b) transfer $I_d - V_{gs}$, and (c) subthreshold $I_d - V_{gs}$ characteristics for InGaAs MOSFET with L_{eff} of 70 nm. The experiment data is shown in black symbols, the MVS model with classical parameters, $R_{sd} = R_{on}(0)$, in dashed blue; and MVS model with ballistic modification in continuous red, $R_{sd} = R_{on}(0) - R_B$.

must be removed from $R_{on}(0)$: $R_{sd} = R_{on}(0) - R_B$. This leads to an external resistance value significantly lower that $R_{on}(0)$: $R_s + R_d = 86\ \Omega.\mu$m.[1]

With this revised estimation of the external resistance, the MVS model yields the characteristics of the $L_{eff} = 70$ nm MOSFET that are shown in solid lines (red) in Fig. 3. The ballistic model predictions now closely reproduce the output, and transfer characteristics, particularly, at high current where the discrepancy with incorrect value of R_{sd} is quite large. It should be noted that no other model device parameter can be tuned in an effort to solve this discrepancy without upsetting the match of the characteristics somewhere else. The input parameters of electron effective mass and non-parabolicity for the MVS model adapted for the InGaAs MOSFET studied here are the same as in [7]. The parameters for source/drain structure accounting for the ballistic resistance, channel mobility, and electrostatics for the MOSFET here are summarized in Table I.

III. Discussion

The impact of ballistic resistance on the device model depends on the device technology being analyzed. The ballistic resistance values at an electron concentration $N_s = 5 \times 10^{12}$ cm^{-2} have been estimated for silicon devices in [5] as well as the devices analyzed in this work. In Table II, the reported experimental value of R_s and the calculated ratio of $R_B/R_{on}(0)$ are given. High $R_B/R_{on}(0)$ suggests a prominent impact of the ballistic resistance. In the self-aligned InGaAs MOSFETs, $R_B/R_{on}(0)$ is the highest with a value of 0.37, at least 30% higher than state-of-the-art silicon transistors. As a result of the advanced extrinsic engineering to reduce external resistances in InGaAs MOSFETs, R_B can be extracted accurately. In this case, the signature of ballistic transport clearly emerges and requires careful separation in a modeling exercise.

[1]This value is 16% higher than the one reported previously in [4] of 74 $\Omega.\mu$m. The difference is small and we attribute it to die-to-die variations.

TABLE I
KEY INPUT PARAMETERS FOR THE MVS MODEL [6], [7]

Parameter	Value
Sum of source and drain resistance, R_s+R_d	86 Ω.μm
Long channel effective mobility, μ_{eff}	Look-up table (see Fig. 1b and text)
Oxide capacitance, C_{ox}	6.9 μF/cm^2
Low-V_g channel charge-centroid equivalent capacitance, C_{QM}	5.3 μF/cm^2
Equilibrium energy difference between the source Fermi level and the first sub-band in the channel, which sets the transistor threshold voltage, E_{fs}-ϵ_{10}	-42 meV
Drain-induced barrier lowering, DIBL	125 mV/V
Non-ideality factor, n_0	1.6

TABLE II
SOURCE RESISTANCE AND THE RATIO $R_B/R_{ON}(0)$ AT $N_s = 5 \times 10^{12}$ CM^{-2} IN DIFFERENT N-CHANNEL FETS

n-FET structure	R_s (Ω.μm)	$R_B/R_{on}(0)$	Ref.
Si ETSOI FETs	115	0.21	[5]
Si FinFETs	75	0.29	[5]
InGaAs MOSFETs	43	0.37	This work

IV. Conclusions

We have discussed the impact of ballistic transport in the physics-based compact modeling of nano-scale transistors. The letter points out that the classically extracted R_{sd} using the R_{on} vs. L_{eff} method is overestimated as it includes the ballistic resistance that is associated with near-equilibrium, linear-region transport in the intrinsic channel. We have shown that this classical approach cannot reproduce adequately the device characteristics of self-aligned InGaAs MOSFETs. Appropriate extraction of R_{sd} accounting for the ballistic resistance, on the other hand, yields an excellent match.

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